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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,382	08/17/2001	Gerard Chauvel	TI-31356	4442

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EXAMINER

KIM, HONG CHONG

ART UNIT	PAPER NUMBER
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2186

DATE MAILED: 03/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/932,382

Applicant(s)

CHAUVEL, GERARD

Examiner

Hong C Kim

Art Unit

2186



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 August 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

Detailed Action

1. Claims 1-13 are presented for examination. This office action is in response to the amendment filed on 8/17/01.
2. Receipt is acknowledged of information disclosure statement filed on 2/14/02, which the statement has been placed of record in the file. Information disclosed and listed on PTO 1449 was considered.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in EPO on 8/21/00 and 5/11/01. It is noted, however, that applicant has not filed a certified copy of the EP 00402331.3 and EP 01401216.5 application as required by 35 U.S.C. 119(b).
4. Applicants are requested to update the status of the related U.S. patent application referred to on page 1 in the specification, accordingly (e.g., U.S. Patent Application Serial No. ####,### filed Sept. 07, 1990, now abandoned; ..., now U.S. Patent #,###,### issued Jan. 01, 1994; or This application is a continuation of Serial Number ####,###, filed on December 01, 1990, now abandoned; ...etc.). Also applicants are requested to include the status of the related U.S. applications or patents in the CROSS-REFERENCE TO RELATED APPLICATIONS section and in any other corresponding area in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-2, 8, and 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al. (Chang) US Patent No. 6,289,414.

As to claim 1, Chang discloses the invention as claimed. Chang discloses a method of operating a digital system having a processor (col. 2 lines 47-48) and associated TLB (col. 3 lines 57-59), comprising the steps of: executing a plurality of program tasks (col. 1 lines 16-23, col. 2 lines 47-49 and col. 22 lines 39-41); initiating a plurality of memory access requests in response to the program tasks (col. 1 lines 16-23, col. 2 lines 47-49 and col. 22 lines 39-41); caching a plurality of translated memory addresses in the TLB in response to the plurality of memory access requests (col. 3 lines 52+, col. 11 lines 21-38 and col. 15 lines 45+); and incorporating a task ID value (Fig. 5 and col. 10 line 35); and locking or unlocking a portion of the plurality of translated memory address in the TLB such that only an entry of a selected program task in the plurality of translated memory addresses is affected (Fig. 5 lock bits and col. 9 lines 48-54).

As to claim 2, Chang further discloses wherein the step of locking or unlocking

comprises locking or unlocking only and all of the plurality of translated addresses that have the selected task id value (col. 10 lines 35-37).

As to claim 8, Chang discloses the invention as claimed. Chang discloses a digital system (col. 2 lines 47-48) having a TLB (col. 3 lines 57-59), comprising: storage circuitry with a plurality of entry locations (Fig. 4) which includes a first field for a translated value (Fig. 5 Ref RPN) and a second field for an associated qualifier value (Fig. 5 Ref. TID and col. 10 lines 35-38); a set of inputs (col. 1 lines 16-23, col. 2 lines 47-49 and col. 22 lines 39-41); a set of output for providing a translated value (col. 3 lines 52+, col. 11 lines 21-38 and col. 15 lines 45+); and control circuitry connected to the storage circuitry, wherein the control circuitry is responsive to an command to lock or unlock selected ones of the plurality of entry locations (Fig. 5 lock bits and col. 9 lines 48-54).

As to claim 10, Chang further discloses wherein each of the plurality of entry locations in the storage circuitry contain a third field (col. 10 lines 18-28).

As to claim 11, Chang further discloses a shift register (abstract, examined for a match with the effective address read on this limitation since each valid entry has to compare in sequence and col. 15 lines 40-43) and skip circuitry (col. 11 lines 58-59, locking /unlocking processing reads on this limitation since locked entry is not available for the access).

As to claim 12, Chang further discloses reservation circuitry (allocation of TLB entries reads on this limitation).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) a patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1-7 and 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond et al. (Hammond) US Patent No. 5,940,872 in view of Mohamed et al. (Mohamed) US Patent No. 5,899,994 or Ganapathy et al. (Ganapathy) US Patent No. 6,182,089.

As to claim 1, Hammond discloses a method of operating a digital system having a processor (col. 1 line 6) and associated TLB (col. 2 lines 3-4), comprising the steps of: executing a program task (col. 2 lines 25+), initiating a plurality of memory access requests in response to the program task. (Col. 2 lines 25+); caching a plurality of translated memory addresses in the TLB in response to the plurality of memory access requests (col. 2 lines 3-4, lines 32-35, and lines 60-63); and locking or unlocking a portion of the plurality of translated memory address in the TLB such that only an entry of a selected program task in the plurality of translated memory addresses is affected (Fig. 6 and col. 6 lines 29-45). However, Hammond does not specifically disclose the step of incorporating a task ID value.

Mohamed discloses the step of incorporating a task ID value (Fig. 7 Ref. 310) for the purpose of running multiple process at the same time (Fig. 5 and col. 6 lines 27-57) thereby increasing the system throughput and decreasing thrashing (col. 6 lines 47-57).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the step of incorporating a task ID value as shown in Mohamed into the invention of Hammond for the advantages stated above.

Alternatively, Ganapathy also discloses the step of incorporating a task ID value (col. 8 lines 46-49) for the purpose of sharing by the multiple processes (col. 6 lines 20-23 and col. 8 lines 46-49) thereby increasing the system throughput.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the step of incorporating a task ID value as shown in Ganapathy into the invention of Hammond for the advantages stated above.

As to claim 2, Hammond, Mohamed, and Ganapathy disclose the invention as claimed in the above. Hammond further discloses wherein the step of locking or unlocking comprises locking or unlocking only and all of the plurality of translated addresses (Fig. 6). Mohamed further discloses task ID value (Fig. 7 Ref. 310). Ganapathy also discloses task ID value (col. 8 lines 46-49).

As to claim 3, Hammond, Mohamed, and Ganapathy disclose the invention as claimed in

the above. Hammond further discloses the TLB has several levels (Col. 8 lines 31-39).

As to claim 4, Hammond, Mohamed, and Ganapathy disclose the invention as claimed in the above. Hammond further discloses a second qualifier (Fig. 2 region ID, key, and rights).

As to claim 5, Hammond, Mohamed, and Ganapathy disclose the invention as claimed in the above. Mohamed further discloses processor identification (Fig. 5).

As to claim 6, Hammond, Mohamed, and Ganapathy disclose the invention as claimed in the above. Hammond further discloses the step of replacing a selected victim translated memory address with different translated memory address (col. 5 lines 51-55).

As to claim 7, Hammond, Mohamed, and Ganapathy disclose the invention as claimed in the above. Hammond further discloses the step of serving a portion of the entry locations being locked (col. 7 lines 25-28).

As to claim 8, Hammond discloses a digital system (col. 1 lines 1-6) having a TLB (col. 2 lines 3-4), comprising: storage circuitry with a plurality of entry locations (Fig. 2) which includes a first field for a translated value (Fig. 2 Ref Physical page No.); a set of inputs (Col. 2 lines 25+); a set of output for providing a translated value (col. 2 lines 3-4, lines 32-35, and lines

60-63); and control circuitry connected to the storage circuitry, wherein the control circuitry is responsive to an command to lock or unlock selected ones of the plurality of entry locations (Fig. 6 and col. 6 lines 29-45). However, Hammond does not specifically disclose a second field for an associated qualifier value.

Mohamed discloses a second field for an associated qualifier value (Fig. 7 Ref. 310) for the purpose of running multiple process at the same time (Fig. 5 and col. 6 lines 27-57) thereby increasing the system throughput and decreasing thrashing (col. 6 lines 47-57).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a second field for an associated qualifier value as shown in Mohamed into the invention of Hammond for the advantages stated above.

Alternatively, Ganapathy also discloses a second field for an associated qualifier value (col. 8 lines 46-49) for the purpose of sharing by the multiple processes (col. 6 lines 20-23 and col. 8 lines 46-49) thereby increasing the system throughput.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a second field for an associated qualifier value as shown in Ganapathy into the invention of Hammond for the advantages stated above.

As to claim 9, Hammond, Mohamed, and Ganapathy disclose the invention as claimed in the above. Hammond further discloses the TLB has several levels (Col. 8 lines 31-39).

As to claim 10, Hammond, Mohamed, and Ganapathy disclose the invention as claimed in the above. Hammond further discloses a third qualifier (Fig. 2 region ID, key, and rights).

As to claim 11, Hammond, Mohamed, and Ganapathy disclose the invention as claimed in the above. Hammond further discloses a shift register (col. 5 lines 55-57) and skip circuitry (col. 6 lines 30-45, locking/unlocking processing reads on this limitation since locked entry is not available for the access).

As to claim 12, Hammond, Mohamed, and Ganapathy disclose the invention as claimed in the above. Hammond further discloses reserving a portion of the entry locations being locked (col. 7 lines 25-28).

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond et al. (Hammond) US Patent No. 5,940,872 in view of Mohamed et al. (Mohamed) US Patent No. 5,899,994 or Ganapathy et al. (Ganapathy) US Patent No. 6,182,089 and further in view of Woolsey et al. (Woolsey) US Patent No. 6,029,000.

As to claim 13, Hammond, Mohamed, and Ganapathy disclose the invention as claimed in the above. However, neither Hammond, Mohamed, nor Ganapathy discloses the digital system being a PDA and further comprises; a processor, a display, radio frequency circuitry, and an aerial connected to the RF circuitry.

Woolsey discloses the digital system being a PDA and further comprises; a processor, a display, radio frequency circuitry, and an aerial connected to the RF circuitry (col. 2 lines 29-44) for the purpose of providing a portability of the system.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the digital system being a PDA and further comprises; a processor, a display, radio frequency circuitry, and an aerial connected to the RF circuitry as shown in Woolsey into the combined invention of Hammond, Mohamed, and Ganapathy for the advantages stated above.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

11. a shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

12. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art

disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).

13. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

14. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matt Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

15. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to TC-2100:

After-Final (703) 746-7238

Official (703) 746-7239 (for formal communications intended for

entry)

Non-Official/Draft (703) 746-7240 (for informal or draft communications, please

label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Primary Patent Examiner
March 13, 2003

